

APR 29 2004

Sheet 1 of 2

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

58269.00014

SERIAL NO.

09/943,238

## LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

APPLICANT

TZENG

FILING DATE

August 31, 2001

GROUP

2661

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

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Technology Center 2600

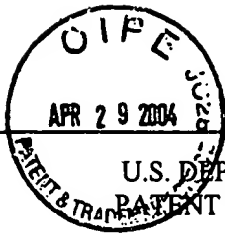
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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION		
							YES	NO	PART.
PB	AG	WO 00/03256	Jan. 20, 2000	WIPO			XX		
	AH								
	AI								
	AJ								
	AK								

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PB	AL	Level One: "Level One™ IXP1200 Network Processor", September 1999, XP002187948, URL: <a href="http://www.cs.utah.edu/cs6935/Previous/s01/netprocs/ixa/ixp1200ad.pdf">http://www.cs.utah.edu/cs6935/Previous/s01/netprocs/ixa/ixp1200ad.pdf</a> , retrieved on Jan. 22, 2002.
PB	AM	Noureddine W et al: "Selective Back-Pressure in Switched Ethernet LANS" 1999 IEEE Global Telecommunications Conference, Globecom '99, Seamless Interconnection for Universal Services, Brazil, IEEE Global Telecommunications Conference, New York, vol. 2, Dec. 5, 1999, pages 1256-1263, XP002258500.
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EXAMINER <i>[Signature]</i>		DATE CONSIDERED 07/15/05

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Sheet 2 of 2

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PB	AL	Mannon P: "10-Gbit Ethernet Switching Processor Blasts Barriers to the Backbone", Electronic Design, Penton Publishing, Cleveland, vol. 48, no. 16, Aug. 7, 2000, pages 72-74, 76, XP001076479.
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FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 023925-00014	SERIAL NO. New Application
<b>LIST OF REFERENCES CITED BY APPLICANT</b>  <i>(Use several sheets if necessary)</i>		APPLICANT TZENG	
		FILING DATE August 31, 2001	GROUP Not yet assigned

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PB	AB	5,644,784	Jul. 1, 1997	Peek			Mar. 3, 1995
PB	AD	5,828,653	Oct. 27, 1998	Goss			Apr. 26, 1996
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PB	AK	5,473,607	Dec. 5, 1995	Hausman et al.			Aug. 9, 1993
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PB	BF	5,898,687	Apr. 27, 1999	Hariman et al.			Jul. 24, 1996
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PB	BP	EP 0 465 090 A1	Jan. 8, 1992	EPO			xx		
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PB	CF	WO 99/00945	Jan. 7, 1999	WIPO			xx		
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PB	CK	"Queue Management for Shared Buffer and Shared Multi-buffer ATM Switches," Yu-Sheng Lin et al., Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C., March 24, 1996, pages 688-695
PB	CL	"A 622-Mb/s 8 x 8 ATM Switch Chip Set with Shared Multibuffer Architecture," Harufusa Kondoh et al., 8107 IEEE Journal of Solid-State Circuits 28(1993) July, No. 7, New York, US, pages 808-814
PB	CM	"Catalyst 8500 CSR Architecture," White Paper XP-002151999, Cisco Systems Inc. 1998, pages 1-19
PB	CN	"Computer Networks," A.S. Tanenbaum, PRENTICE-HALL INT., USA, XP-002147300(1998), Sec. 5.2-Sec. 5.3, pages 309-320

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